The documentation and process conversion measures necessary to comply with this revision shall be completed by 7 November 2015.

INCH-POUND

MIL-PRF-19500/369J
7 August 2015
SUPERSEDING
MIL-PRF-19500/369H
15 July 2010

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, NPN, SILICON, POWER,
TYPE 2N3441, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for NPN, silicon, power transistor. Three levels of product assurance are provided for each device type (JAN, JANTX, and JANTXV).

* 1.2 Package outlines. The device package outlines are as follows: similar to TO-66 in accordance with figure 1 for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C.

P_T		$R_{\theta JA}$	$R_{\theta JC}$	V_{CBO}	V_{CEO}	V_{EBO}	V_{CER}	I_B	I_C	T_{STG} and T_J
T_A = +25°C (1)	T_C = +25°C (1)		(2)							
W	W	°C/W	°C/W	V dc	V dc	V dc	V dc	A dc	A dc	°C
3.0	25	58.5	3	160	140	7.0	150	2.0	3.0	-65 to +200

(1) For derating see figures 2 and 3.
(2) For thermal impedance see figure 4.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A

FSC 5961

1.4 Primary electrical characteristics. Unless otherwise specified, T_A = +25°C.

	h_{FE2} V_{CE} = 4 V dc I_C = 0.5 A dc	$\|h_{fe}\|$ V_{CE} = 4 V dc I_C = 0.5 A dc f = 100 kHz	h_{fe} V_{CE} = 4 V dc I_C = 0.5 A dc	$V_{CE(sat)}$ I_C = 0.5 A dc I_B = 50 mA dc	Pulse response	
					t_{on}	t_{off}
				V dc	µs	µs
Min	25	4	15			
Max	100	40	100	1	8	15

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JAN”, “JANTX”, and "JANTXV".

* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.2.2 Second number symbols. The second number symbol for the transistor covered by this specification sheet is as follows: "3441".

* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

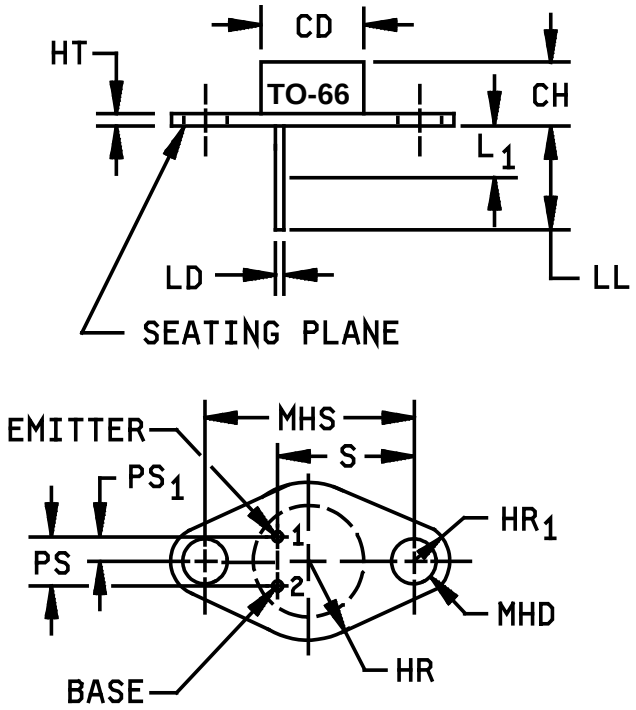


FIGURE 1. Physical dimensions (similar to TO-66).

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.470	.500	11.94	12.70	
CH	.250	.340	6.35	8.64	
HR		.350		8.89	
HR_1	.115	.145	2.92	3.68	
HT	.050	.075	1.27	1.91	
LD	.028	.034	0.71	0.86	4, 6
LL	.360	.500	9.14	12.70	
L_1		.050		1.27	6
MHD	.142	.152	3.61	3.86	4
MHS	.958	.962	24.33	24.43	
PS	.190	.210	4.83	5.33	3
PS_1	.093	.107	2.36	2.72	3
S	.570	.590	14.48	14.99	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. These dimensions should be measured at points .050 inch (1.27 mm) +.005 inch (0.13 mm) - 0 inch below seating plane. When gauge is not used, measurement will be made at the seating plane.
4. Two places.
5. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
6. Lead diameter shall not exceed twice LD within L_1.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
8. Pin 1 is the emitter and pin 2 is the base. The collector shall be electrically connected to the case.

FIGURE 1. Physical dimensions - Continued.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement JANTX and JANTXV levels
(1) 3c	Thermal impedance, see 4.3.2.
9	Not applicable.
11	I_{CEX1} and h_{FE3} .
12	Burn-in (see 4.3.1).
13	ΔI_{CEX1} = 100 percent of initial value or 2 μA whichever is greater. Δh_{FE3} = ±25 percent Subgroup 2 table I herein.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:

T_A = +30°C ±5°C, $V_{CB} \geq$ 100 V dc., T_J = +187.5°C ±12.5°C.

NOTE: No heatsink or forced air-cooling on the devices shall be permitted.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table II, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500, and as follows.

Subgroup	Method	Conditions
B3	1027	T_J = +187.5°C ±12.5°C, T_A = +25°C ±5°C; V_{CB} > 24 V dc.
B6	1032	T_{STG} = +200°C
B7	3053	Load condition C; (unclamped inductive load), (see safe operating area figure herein) T_C = +25°C, duty cycle ≤ 10 percent, R_1 = 0.1 Ω, $t_r = t_f \leq 500$ ns. Test 1. tp = 10 ms, (vary to obtain I_G), V_{BB2} = 1.5 V dc, R_{BB1} = 5 Ω, L = 5 mH (two Super Electric Corporation type S16884 in parallel or equivalent, dc resistance ≤ 0.1 Ω), V_{BB1} = 10 V, R_{BB2} = 100 Ω, V_{CC} = 10 V dc, I_C = 3 A dc. Test 2. tp = 10 ms, (vary to obtain I_C), V_{BB2} = 1.5 V dc, R_{BB1} = 50 Ω, L = 100 mH (two Traid C48U in series: 80 mH winding and 20 mH winding or equivalent, dc resistance ≤ 0.1 Ω), V_{BB1} = 10 V, R_{BB2} = 100 Ω, V_{CC} = 10 V dc, I_C = 0.5 A dc.
B7	3053	Load condition B (see safe operating figure herein), T_A = +25°C, L = 20 mH (Traid C48U or equivalent, dc resistance ≤ 0.1 Ω), V_{CC} = 50 V dc, I_C = 3 A dc, R_{BB1} = 5 Ω, V_{BB1} = 10 V dc, clamped voltage = 140 V dc, R_{BB2} = 100 Ω, V_{BB2} = 1.5 V dc.

* 4.4.3 Group C inspection, Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows.

Subgroup	Method	Conditions
C2	1056	Test condition B.
C2	2036	Test condition A, weight - 3 pounds, 15 seconds.
C5	3131	Thermal resistance, see 4.3.2, $R_{\theta JC}$ = 3°C/W.
C6	1026	T_J = +187.5°C ±12.5°C, T_A = +25°C ±5°C, $V_{CB} \geq$ 24 V dc.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2.

4.5 Methods of inspection. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 2/	3131	See 4.3.2.	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to base	3011	Bias condition D, pulsed (see 4.5.1), I_C = 100 mA dc	$V_{(BR)CEO}$	140		V dc
Breakdown voltage, collector to emitter	3011	Bias condition B, I_C = 100 mA dc, R_{BE} = 100Ω, pulsed (see 4.5.1)	$V_{(BR)CER}$	150		V dc
Breakdown voltage, collector to emitter	3011	Bias condition A, I_C = 100 mA dc, V_{BE} = -1.5 V dc, pulsed (see 4.5.1)	$V_{(BR)CEX}$	160		V dc
Emitter to base current	3061	Bias condition D, V_{EB} = 7.0 V dc	I_{EBO}		1	mA dc
Collector - emitter cutoff current	3041	Bias condition A, V_{BE} = -1.5 V dc, V_{CE} = 140 V dc	I_{CEX1}		20	µA dc
Base emitter voltage (nonsaturated)	3066	Test condition B; pulsed (see 4.5.1), I_C = 0.5 A dc, V_{CE} = 4.0 V dc	V_{BE}		1.7	V dc
Collector to emitter voltage (saturated)	3071	Pulsed (see 4.5.1), I_C = 0.5 A dc, I_B = 50 mA dc	$V_{CE(sat)}$		1	V dc
Forward current transfer ratio	3076	V_{CE} = 4 V dc, I_C = 50 mA dc, pulsed (see 4.5.1)	h_{FE1}	50		
Forward current transfer ratio	3076	V_{CE} = 4 V dc, I_C = 0.5 A dc, pulsed (see 4.5.1)	h_{FE2}	25	100	
Forward current transfer ratio	3076	V_{CE} = 4 V dc, I_C = 1 A dc, pulsed (see 4.5.1)	h_{FE3}	10		

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High temperature operation:		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A, V_{BE} = -1.5 V dc, V_{CE} = 140 V dc	I_{CEX}		5	mA dc
Low temperature operation		T_A = -65°C				
Forward current transfer ratio	3076	V_{CE} = 4 V dc, I_C = 0.5 A dc, pulsed (see 4.5.1)	h_{FE4}	15		
Subgroup 4						
Pulse response transfer ratio	3251	Test condition A, except test circuit and pulse requirements in accordance with figure 5 herein.				
Turn-on time		V_{CC} = 30 V dc, (see figure 5); I_C = 0.5 A dc, I_B = 50 mA dc	t_{on}		8	µs
Turn-off time		V_{CC} = 30 V dc, (see figure 5); I_C = 0.5 A dc, I_{B1} = -I_{B2} = 50 mA dc	t_{off}		15	µs
Magnitude of common emitter small-signal short-circuit forward current transfer ratio	3306	V_{CE} = 4 V dc, I_C = 0.5 A dc, f = 100 kHz	$\|h_{fe}\|$	4	40	
Open circuit (output capacitance)	3236	V_{CB} = 10 V dc, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{obo}		300	pF
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = 4 V dc, I_C = 0.5 A dc, f = 1.0 kHz.	h_{fe}	15	100	

See footnote at end of table.

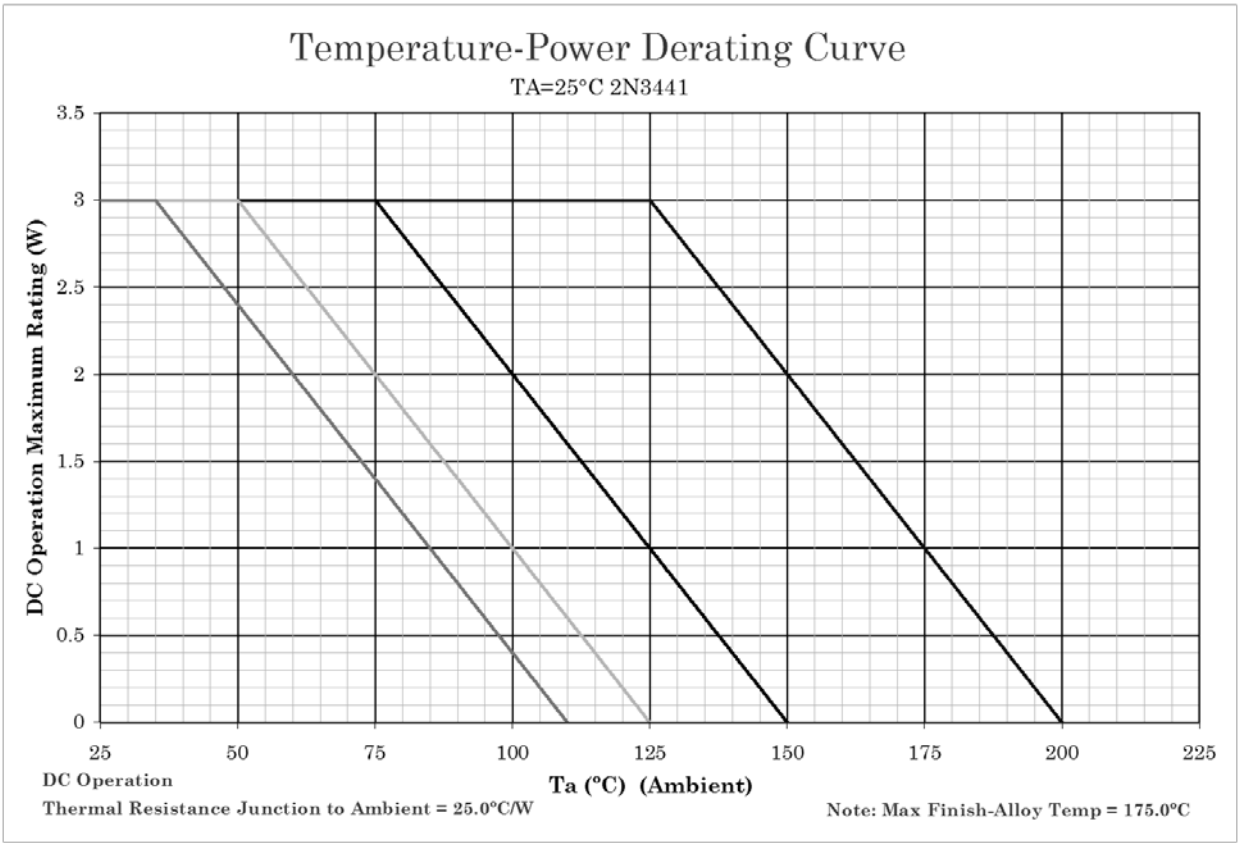
TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area (dc operation)	3051	T_C = +25°C, t = 1 s, 1 cycle, see figure 6 and 7.				
Test 1		I_C = 3 A dc, V_{CE} = 8.33 V dc				
Test 2		I_C = 833 mA dc, V_{CE} = 30 V dc				
Test 3		I_C = 178.5 mA dc, V_{CE} = 140 V dc				
Electrical measurements		See table I, subgroup 2 herein.				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JAN, JANTX and JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group E inspection (all quality levels) for qualification only.

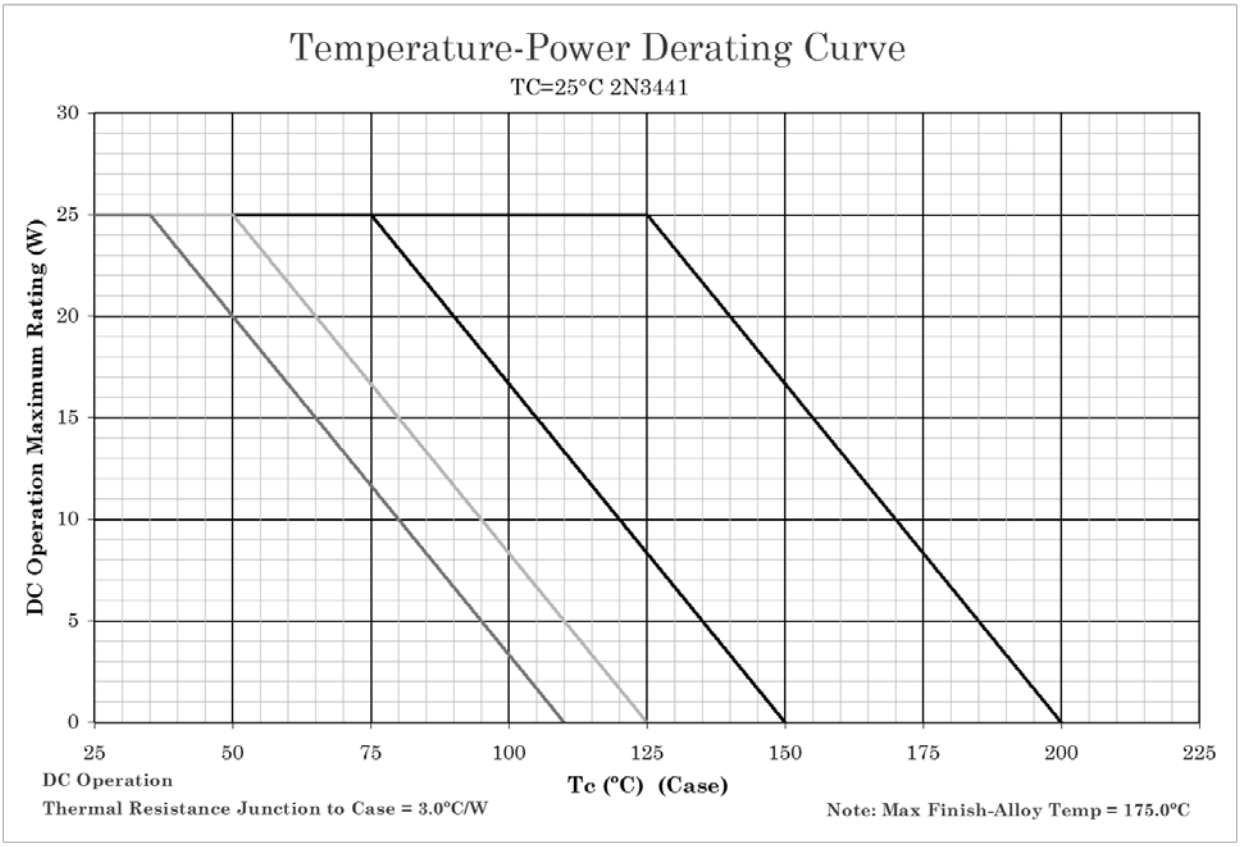
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices, c = 0
Temperature cycling	1051	500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2.	
Subgroup 2			45 devices, c = 0
Blocking life	1048	Test temperature = +125°C; V_{CB} = 80 percent of rated, T = 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C and +110°C to show power rating where most users want to limit T_J in their application.

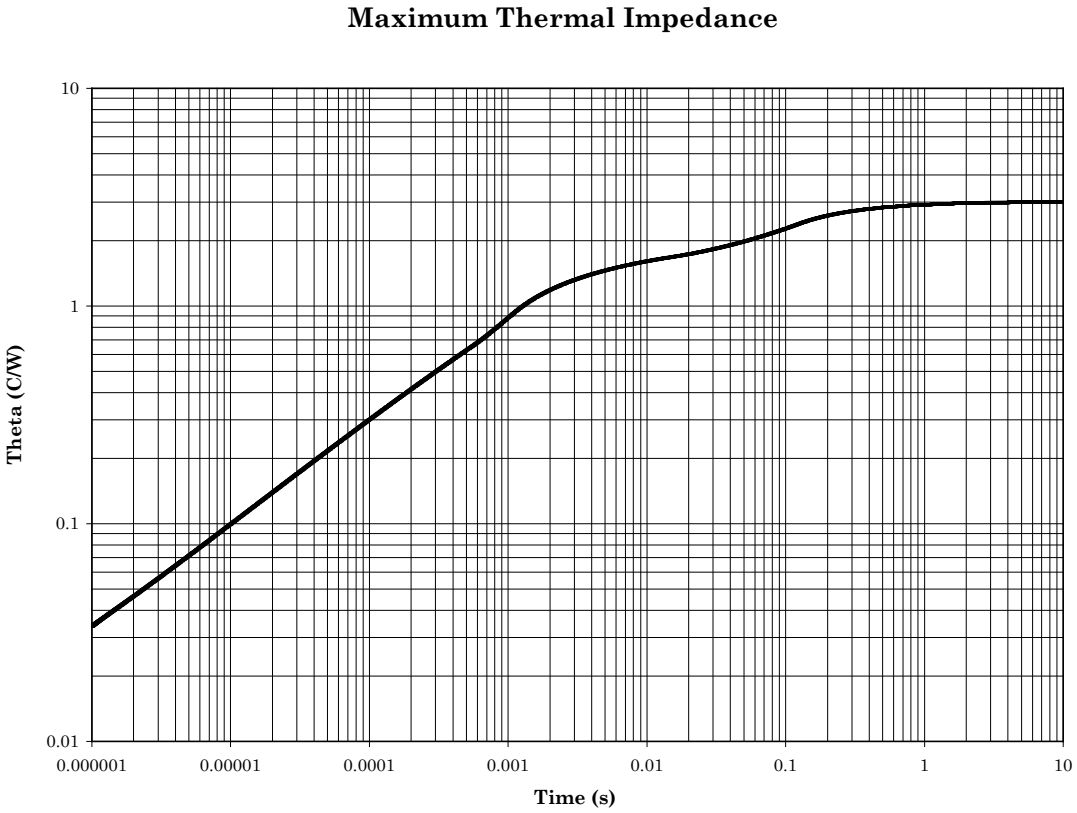
FIGURE 2. Temperature-power derating for 2N3441, $R_{\theta JA}$ = 25°C/W (TO-66).



NOTES:

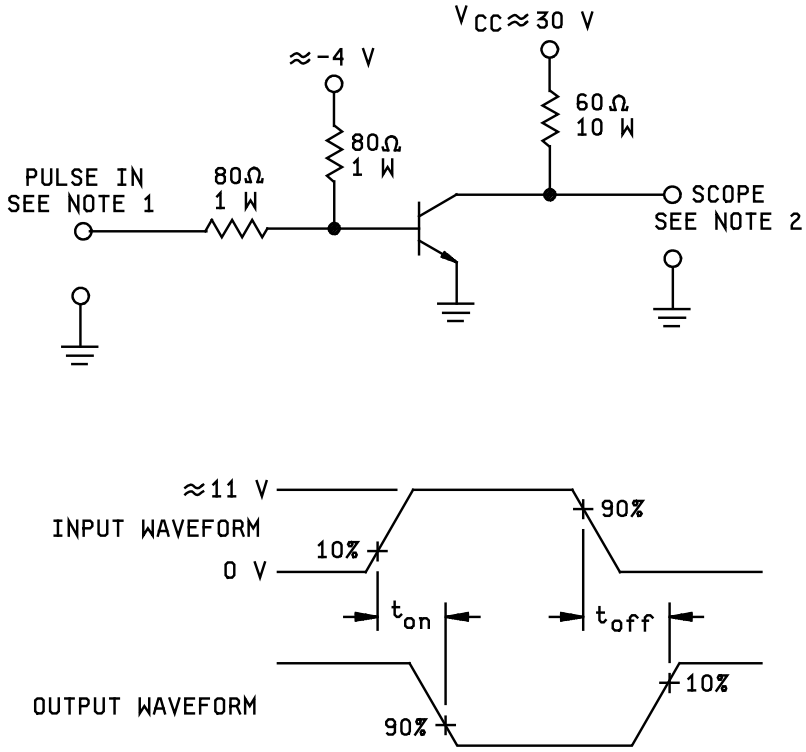
1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 3. Temperature-power derating for 2N3441, $R_{\theta JC}$ = 3°C/W (TO-66).



T_C = +25°C, thermal resistance $R_{\theta JC}$ = 3°C/W at T_C +25°C.

FIGURE 4. Thermal impedance graph for 2N3441, (TO-66).



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be each ≤ 20 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50Ω; pulse width = 20 μs.
2. Output sampling oscilloscope: Z_{in} ≥ 100 kΩ; C_{in} ≤ 50 pF; rise time ≤ 20 ns.

FIGURE 5. Pulse response test circuit.

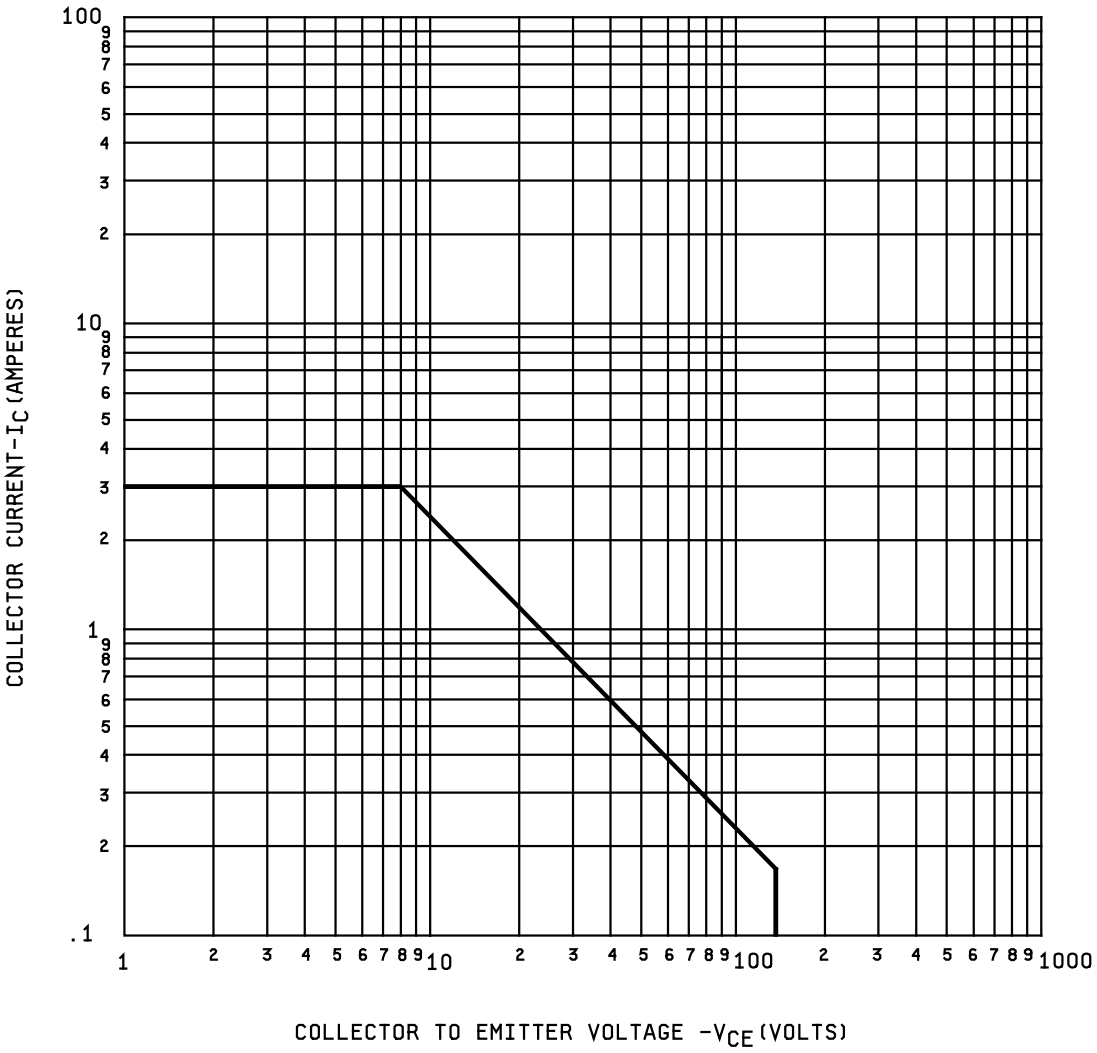


FIGURE 6. Maximum safe operating area graph (continuous dc).

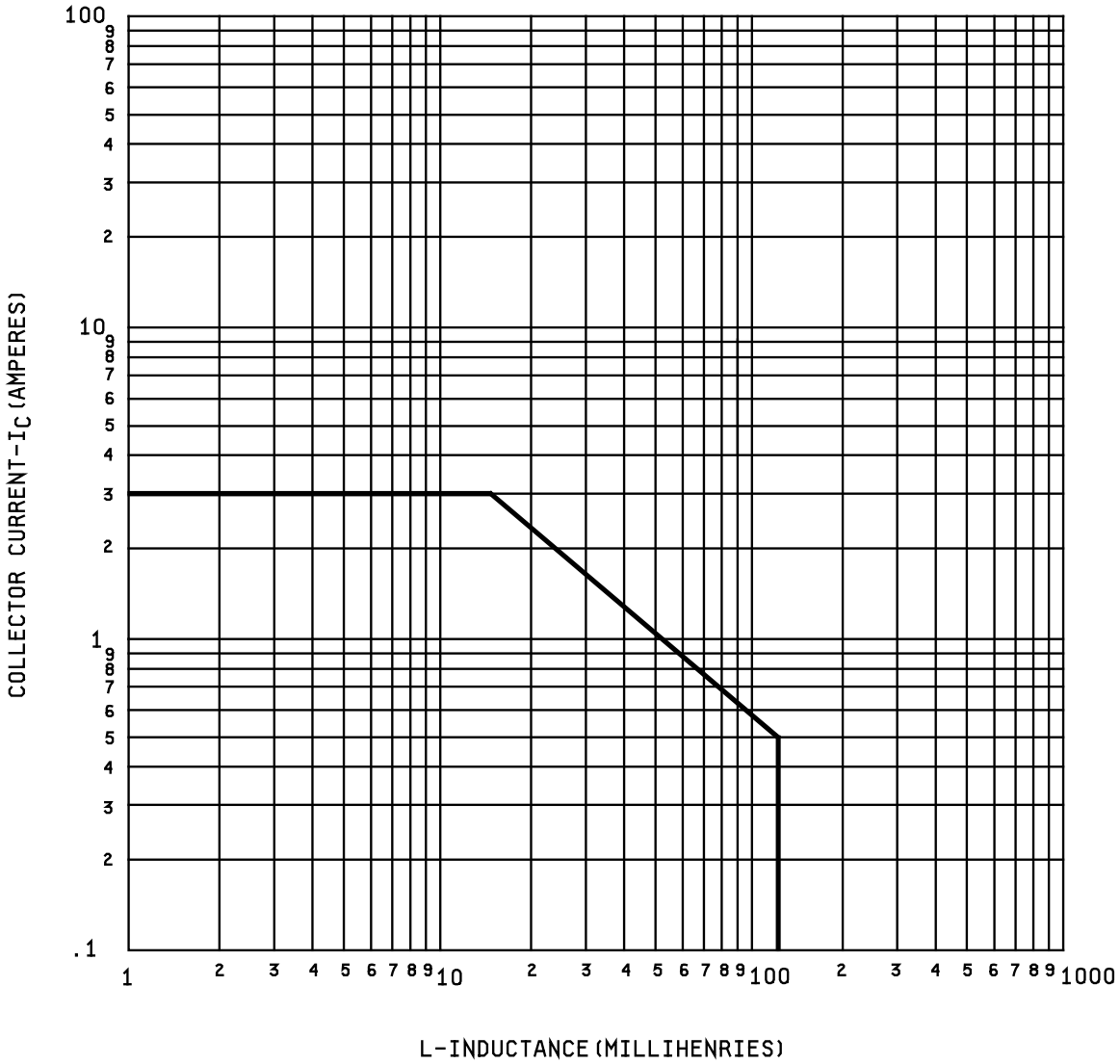


FIGURE 7. Safe operating area for switching between saturation and cutoff (unclamped inductive load) see subgroup 5 of table I.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

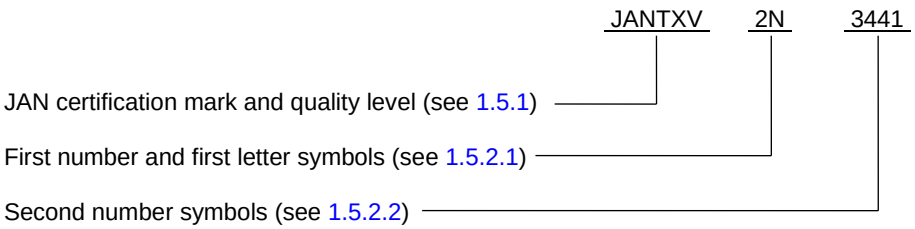
c. Lead finish (see 3.4.1).

* d. The complete Part or Identifying Number (PIN), see 1.5 and 6.4.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

* 6.4 PIN construction example.

* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for types 2N3441
JAN2N3441
JANTX2N3441
JANTXV2N3441

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC

Review activities:
Army - AR, MI, SM
Navy - AS, OS, SH
Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2015-083)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.